DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/05/2011 has been entered.

Claims 3-5, 14-17, 20-21, 36-35, 47-59 are cancelled.

Claims 1-2, 6-13, 18-19, 22-35 and 46 are still pending.

The independent claims 1, 18, 35 and 46 amended the features “a plurality of transparent layers including light-shielding color filter patterns, ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer, the light-shielding color filter patterns including at least two of red, green or blue color resins, the light-shielding color filter patterns having a second top surface”, which is obviously rejected by the references of Miyazaki et al. (US5757451A) with Figure 2 and anticipated by Kadota et al. (US 6031512A).

Claim Rejections - 35 USC § 102

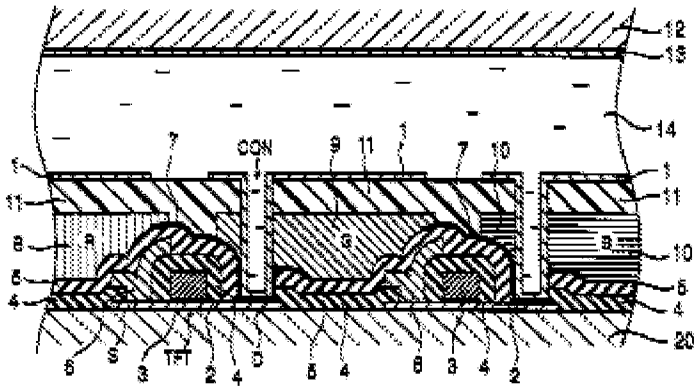
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Kadota et al. (US 6031512A) *with Figure 5 disclose ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer, the light-shielding color filter patterns including at least two of red, green or blue color resins, which partially overlap (**considered as light shield color filter patterns**) the thin film transistor at the same level.*

1. Claims 1, 6-12, 18, 22-31, 35 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by **Kadota et al. (US 6031512A)**.

FIG. 5
(PRIOR ART)



Kadota et al. teach (Figs. 2-3) a liquid crystal display device comprising:

Claims 1, 18, 35 and 46:

- a plurality of gate lines formed on a first substrate along a transverse direction, each gate line including a gate electrode;
- a first insulating layer formed on the first substrate to cover the gate lines and the gate electrodes;
- a plurality of data lines formed on the first insulating layer along a longitudinal direction, the data lines defining a plurality of pixel regions with the gate lines and each including a source electrode;
- a thin film transistor formed at a crossing region of each of the gate and data lines, each thin film transistor including one of the gate electrodes, a semiconductor layer, one of the source electrodes, and a drain electrode;
- a color filter 8 over the first insulating layer in each pixel region, each color filter having one of red, green and blue colors R/G/B, the color filters having a plurality of drain contact holes exposing the drain electrodes; each color filter having a first top surface;
- a pixel electrode 1 over a the first top surface in each pixel region, each pixel electrode contacting one of the drain electrodes through the drain contact hole, wherein a portion of the pixel electrode in the drain contact hole contacts inner side surfaces of the color filter defining the drain contact hole (see Figure 2);
- a common electrode 13 on a second substrate 16, the common electrode facing the first substrate; and
- a liquid crystal layer 14 interposed between the common electrode and the pixel electrodes.

- a plurality of transparent layers 8/11/1 including light-shielding color filter patterns, ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer, the light-shielding color filter patterns including at least two of red, green or blue color resins, the light-shielding color filter patterns having a second top surface,

wherein

- a thickness of the light-shielding color filter patterns is equal to or less than a thickness of the color filter,
- the first and second top surfaces face the common electrode and have the same level of the surface of the flattening film 11.

Claims 1 and 22:

- the light-shielding color filter patterns are formed of the same material as the color filters.

Claims 6 and 23:

- a cell gap between the light-shielding color filter patterns and the common electrode is greater than zero.

Claims 7 and 24:

- the color filters are formed of a photosensitive resin through a photolithography process.

Claims 8 and 25:

- red, green and blue color filters are formed sequentially from the semiconductor layers towards the liquid crystal layer.

Claims 9 and 26:

- each of red, green and blue color filter patterns (at shielding regions) has a thickness smaller than each of red, green and blue color filters (at display regions).

Claims 10 and 27:

- each light-shielding color filter pattern has a red color filter pattern, a green color filter pattern and a blue color filter pattern.

Claims 11 and 28-29:

- a second insulating layer 5 between the thin film transistors and the light-shielding patterns (color filters) and between the first insulating layer (gate insulating film 4 and the color filters, wherein the second insulating layer 11 covers the source electrodes, the drain electrodes 7 and the data lines and wherein the drain contact holes extend through the second insulating layer 5 wherein performing etching an exposed portion of the second insulating layer such that the drain contact holes extend through the second insulating layer to expose a portion of each drain electrode.

Claims 12 and 30-31:

- a third insulating layer (a flattened film 11) between the color filters and the pixel electrodes, wherein the third insulating layer 11 covers the color filters and the light-shielding color filter patterns, wherein performing etching a portion of the third insulating layer corresponding to the drain contact holes such that the drain

contact holes extend through the third insulating layer to expose a portion of each drain electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The secondary reference Midorikawa et al. (US 6281955 B1) *disclose the plurality of pixel electrodes 30 formed directly on top surfaces of the plurality of color filters 24;* ***Midorikawa et al. fail to*** *disclose "the first and second top surfaces face the common electrode and have the same level". However, the primary reference Yamamoto et al. (US6445432B2) discloses "the first and second top surfaces face the common electrode and have the same level".*

1. Claims 1, 6-12, 18, 22-31, 35 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of Midorikawa et al. (US 6281955 B1) and **Miyazaki et al. (US5757451A)**.

Yamamoto et al. teach (Figs. 2-4) a liquid crystal display device comprising:

Claims 1, 18, 35 and 46:

- a plurality of gate lines 3a formed on a first substrate along a transverse direction, each gate line including a gate electrode 3;

- a first insulating layer (gate insulating layer 4) formed on the first substrate to cover the gate lines and the gate electrodes;
- a plurality of data lines 6a formed on the first insulating layer along a longitudinal direction, the data lines defining a plurality of pixel regions with the gate lines and each including a source electrode 6;
- a thin film transistor formed at a crossing region of each of the gate and data lines, each thin film transistor including one of the gate electrodes, a semiconductor layer 5, one of the source electrodes, and a drain electrode;
- a color filter R over the first insulating layer in each pixel region, each color filter having one of red, green and blue colors R/G/B, the color filters having a plurality of drain contact holes exposing the drain electrodes 7; each color filter having a first top surface;
- a pixel electrode 15 over a the first top surface in each pixel region, each pixel electrode contacting one of the drain electrodes through the drain contact hole, wherein a portion of the pixel electrode in the drain contact hole contacts inner side surfaces of the color filter defining the drain contact hole (see Figure 2 below);
- a common electrode on a second substrate 16, the common electrode facing the first substrate; and
- a liquid crystal layer 20 interposed between the common electrode and the pixel electrodes.

- plurality of transparent layers (color filters) including light shielding color filter patterns and the black resin filling a space between the thin film transistor and the liquid crystal layer 20, the light shield color filter color patterns including at least two of red, green or blue resins, the light-shielding color filter patterns having a second top surface,

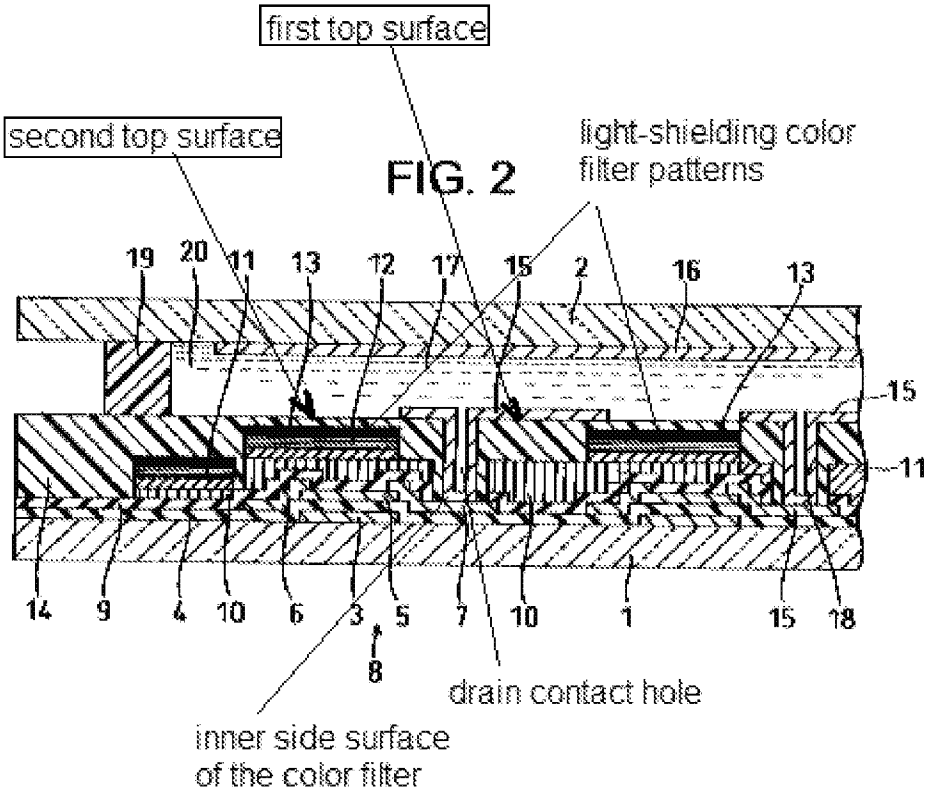


FIG. 2

wherein

- a thickness of the light-shielding color filter patterns is equal to or less than a thickness of the color filter,
- the first and second top surfaces face the common electrode and have the same level of the surface of the flattening film 14.

Claims 1 and 22:

- the light-shielding color filter patterns are formed of the same material as the color filters.

Claims 6 and 23:

- a cell gap between the light-shielding color filter patterns and the common electrode is greater than zero.

Claims 7 and 24:

- the color filters are formed of a photosensitive resin through a photolithography process.

Claims 8 and 25:

- red, green and blue color filters are formed sequentially from the semiconductor layers towards the liquid crystal layer.

Claims 9 and 26:

- each of red, green and blue color filter patterns (at shielding regions) has a thickness smaller than each of red, green and blue color filters (at display regions).

Claims 10 and 27:

- each light-shielding color filter pattern has a red color filter pattern, a green color filter pattern and a blue color filter pattern.

Claims 11 and 28-29:

- a second insulating layer 9 between the thin film transistors 5 and the light-shielding patterns and between the first insulating layer 4 and the color filters, wherein the second insulating layer 9 covers the source electrodes 6, the drain

electrodes 7 and the data lines and wherein the drain contact holes extend through the second insulating layer 9 wherein performing etching (Fig. 3C) an exposed portion of the second insulating layer such that the drain contact holes extend through the second insulating layer to expose a portion of each drain electrode.

Claims 12 and 30-31:

- a third insulating layer (a flattened film 14) between the color filters and the pixel electrodes, wherein the third insulating layer 14 covers the color filters and the light-shielding color filter patterns, wherein performing etching a portion of the third insulating layer corresponding to the drain contact holes such that the drain contact holes extend through the third insulating layer to expose a portion of each drain electrode.

However, Yamamoto et al. fail to disclose (a) the plurality of pixel electrodes are formed directly on top surfaces of the plurality of color filters; (b) ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer.

Midorikawa et al. (US 6281955 B1) teach (Fig. 1) the plurality of pixel electrodes 30 formed directly on top surfaces of the plurality of color filters 24 for obtaining high quality color images due to reducing the electrical coupling between color filter and TFT (col. 2 lines 45-48).

Miyazaki et al. teach (Fig. 2) ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer for enhancing an opening rate with a recent high demand for increasing the luminance of the liquid crystal display device (col. 7 lines 12-14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yamamoto et al. disclosed with (a) the plurality of pixel electrodes formed directly on top surfaces of the plurality of color filters for obtaining high quality color images due to reducing the electrical coupling between color filter and TFT (col. 2 lines 45-48) as Midorikawa et al. taught; (b) ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer for enhancing an opening rate with a recent high demand for increasing the luminance of the liquid crystal display device (col. 7 lines 12-14) **Miyazaki et al.** taught.

*In the following 103-rejection, both primary reference Yamamoto et al. (US6445432B2) and secondary reference **Yanai (US 6137552 A)** disclose "the first and second top surfaces face the common electrode and have the same level".*

2. Claims 1, 6-12, 18, 22-31, 35 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of Yanai (US6137552A) and **Miyazaki et al. (US5757451A)**.

Yamamoto et al. teach (Figs. 2-4) a liquid crystal display device comprising:

Claims 1, 18, 35 and 46:

- a plurality of gate lines 3a formed on a first substrate along a transverse direction, each gate line including a gate electrode 3;
- a first insulating layer (gate insulating layer 4) formed on the first substrate to cover the gate lines and the gate electrodes;
- a plurality of data lines 6a formed on the first insulating layer along a longitudinal direction, the data lines defining a plurality of pixel regions with the gate lines and each including a source electrode 6;
- a thin film transistor formed at a crossing region of each of the gate and data lines, each thin film transistor including one of the gate electrodes, a semiconductor layer 5, one of the source electrodes, and a drain electrode;
- a color filter R over the first insulating layer in each pixel region, each color filter having one of red, green and blue colors R/G/B, the color filters having a plurality of drain contact holes exposing the drain electrodes 7; each color filter having a first top surface;
- a pixel electrode 15 over a the first top surface in each pixel region, each pixel electrode contacting one of the drain electrodes through the drain contact hole, wherein a portion of the pixel electrode in the drain contact hole contacts inner side surfaces of the color filter defining the drain contact hole (see Figure 2 below);
- a common electrode on a second substrate 16, the common electrode facing the first substrate; and

- a liquid crystal layer 20 interposed between the common electrode and the pixel electrodes.
- plurality of transparent layers (color filters) including light shielding color filter patterns and the black resin filling a space between the thin film transistor and the liquid crystal layer 20, the light shield color filter color patterns including at least two of red, green or blue resins, the light-shielding color filter patterns having a second top surface,

wherein

- a thickness of the light-shielding color filter patterns is equal to or less than a thickness of the color filter,
- the first and second top surfaces face the common electrode and have the same level of the surface of the flattening film 14.

Claims 1 and 22:

- the light-shielding color filter patterns are formed of the same material as the color filters.

Claims 6 and 23:

- a cell gap between the light-shielding color filter patterns and the common electrode is greater than zero.

Claims 7 and 24:

- the color filters are formed of a photosensitive resin through a photolithography process.

Claims 8 and 25:

- red, green and blue color filters are formed sequentially from the semiconductor layers towards the liquid crystal layer.

Claims 9 and 26:

- each of red, green and blue color filter patterns (at shielding regions) has a thickness smaller than each of red, green and blue color filters (at display regions).

Claims 10 and 27:

- each light-shielding color filter pattern has a red color filter pattern, a green color filter pattern and a blue color filter pattern.

Claims 11 and 28-29:

- a second insulating layer 9 between the thin film transistors 5 and the light-shielding patterns and between the first insulating layer 4 and the color filters, wherein the second insulating layer 9 covers the source electrodes 6, the drain electrodes 7 and the data lines and wherein the drain contact holes extend through the second insulating layer 9 wherein performing etching (Fig. 3C) an exposed portion of the second insulating layer such that the drain contact holes extend through the second insulating layer to expose a portion of each drain electrode.

Claims 12 and 30-31:

- a third insulating layer (a flattened film 14) between the color filters and the pixel electrodes, wherein the third insulating layer 14 covers the color filters and the light-shielding color filter patterns, wherein performing etching a portion of the

third insulating layer corresponding to the drain contact holes such that the drain contact holes extend through the third insulating layer to expose a portion of each drain electrode.

However, Yamamoto et al. fail to disclose (a) the plurality of pixel electrodes are formed directly on top surfaces of the plurality of color filters; (b) ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer.

Yanai teach (Figs 3-4) the plurality of pixel electrodes 13 formed directly on top surfaces of the plurality of color filters 10 [wherein the first and second top surfaces face the common electrode and have the same level].

FIG. 3

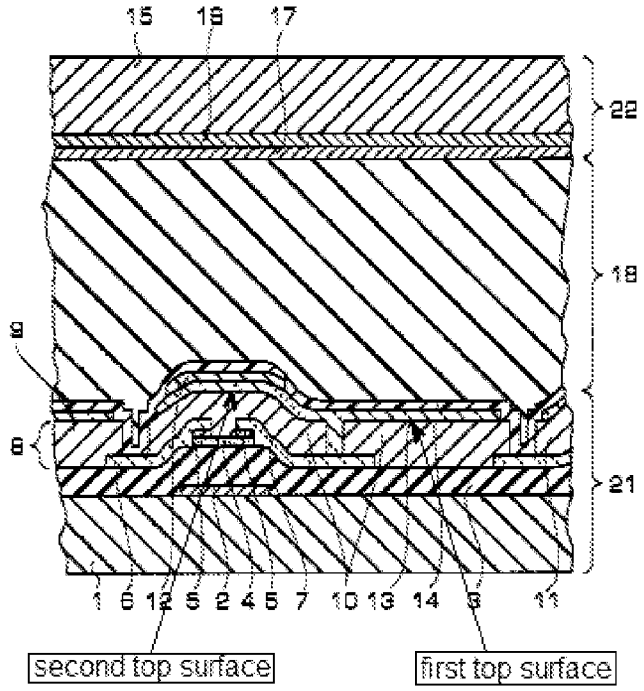
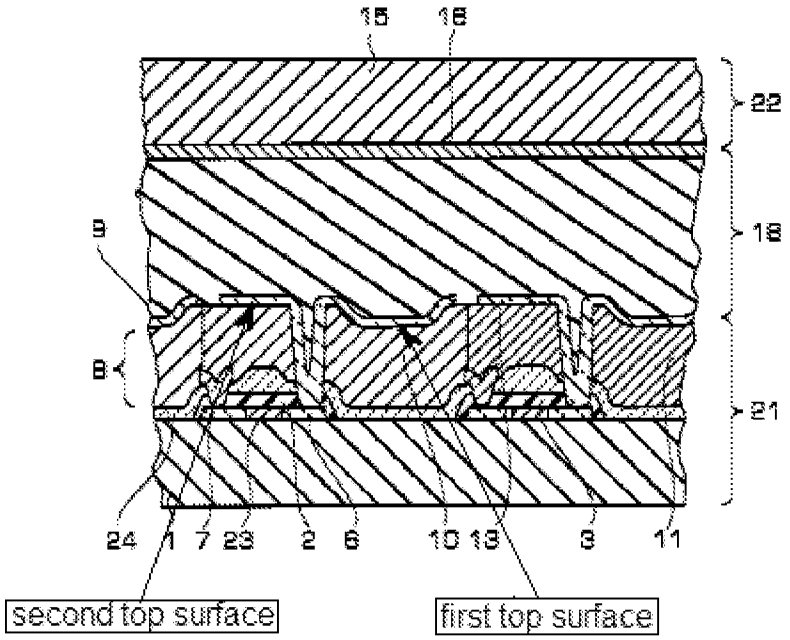


FIG. 4
PRIOR ART



Miyazaki et al. teach (Fig. 2) ONLY the plurality of transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer for enhancing an opening rate with a recent high demand for increasing the luminance of the liquid crystal display device (col. 7 lines 12-14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yamamoto et al. disclosed with (a) the plurality of pixel electrodes formed directly on top surfaces of the plurality of color filters for improving in its brightness by increasing its aperture ratio while preventing a malfunction of TFTs due to incidence of rays from an external light on a back channel of the TFTs (abstract); (b) ONLY the plurality of

transparent layers without any black matrix filling a space between the thin film transistor and the liquid crystal layer for enhancing an opening rate with a recent high demand for increasing the luminance of the liquid crystal display device (col. 7 lines 12-14) **Miyazaki et al.** taught.

3. Claims 2 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of Midorikawa et al. (US 6281955 B1) [or Yanai (US 6137552 A)] and **Miyazaki et al. (US5757451A)** as applied to claims 1, 6-12, 18, 22-31 and 35 and in further view of Shin (US5825449A).

Yamamoto et al. fail to disclose a liquid crystal display device comprising the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer between the source and drain electrodes as cited in claims 2 and 19.

Shin teaches (Figs. 2-3) a liquid crystal display device comprising the source and drain electrodes are formed on the ohmic contact layer 5 and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer 4 between the source and drain electrodes for reducing the contact resistance between the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as

Yamamoto et al. disclosed with the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer between the source and drain electrodes for reducing the contact resistance between the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).

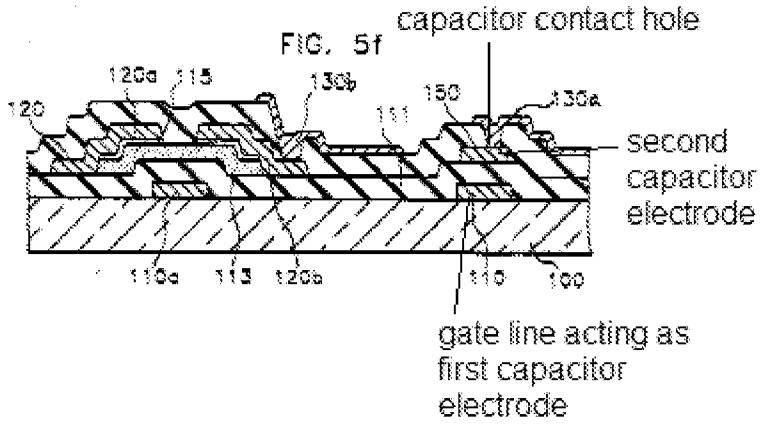
4. Claims 13 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of Midorikawa et al. (US 6281955 B1) [or Yanai (US 6137552 A)] and **Miyazaki et al. (US5757451A)** as applied to claims 1, 6-12, 18, 22-31 and 35 and in further view of Song (US6307602B1).

Yamamoto et al. further disclose a liquid crystal display device comprising colors filters covering gate lines.

Yamamoto et al. fail to disclose a liquid crystal display device comprising a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode on the first insulating layer over each portion of the gate line, wherein each second capacitor electrode and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode. Each color filter includes a capacitor contact hole exposing one of the second capacitor electrodes and wherein the pixel electrodes contacts the second capacitor electrodes through the capacitor contact holes.

Song teaches (Fig. 4a-5f) a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode 150 on the first insulating layer (gate

insulating layer 111) over each portion of the gate line, wherein each second capacitor electrode 150 and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode. The passivation layer 117 includes a capacitor contact hole exposing one of the second capacitor electrodes and wherein the pixel electrodes contacts the second capacitor electrodes through the capacitor contact holes.



Combination of **Yamamoto et al.** and Song (Figs. 4-5 show storage electrodes covering gate lines) is obviously replaced the passivation layer by color filters for each pixel, which should includes capacitor contact hole exposing the second capacitor electrode, wherein the pixel electrode contact the second capacitor electrodes through the capacitor contact holes.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yamamoto et al. disclosed with a portion of each gate line acts as a first capacitor

electrode and a second capacitor electrode 150 on the first insulating layer (gate insulating layer 111) over each portion of the gate line, wherein each second capacitor electrode 150 and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode The color filter includes a capacitor contact hole exposing one of the second capacitor electrodes and wherein the pixel electrodes contacts the second capacitor electrodes through the capacitor contact holes for high display quality with preventing shorting between pixel electrodes as Song taught (col. 2 lines 25-34).

5. Claims 2 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over **Kadota et al. (US 6031512A)** as applied to claims 1, 6-12, 18, 22-31 and 35 in view of Shin (US5825449A).

Kadota et al. fail to disclose a liquid crystal display device comprising the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer between the source and drain electrodes as cited in claims 2 and 19.

Shin teaches (Figs. 2-3) a liquid crystal display device comprising the source and drain electrodes are formed on the ohmic contact layer 5 and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer 4 between the source and drain electrodes for reducing the contact resistance between

the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as **Kadota et al.** disclosed with the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer between the source and drain electrodes for reducing the contact resistance between the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN NGUYEN whose telephone number is (571)272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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